08 512505

APPLICATION
for
UNITED_STATES_ LETTERS_ PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that:
Lizy Kurian John,
residing at 1318 thomasville Circle, Apt. C,
Tampa, County of Hillsborough, State of Florida
a citizen of the United States of America

has invented a new and useful Computer Memory Chip with Field Programmable Memory Cell Arrays (FPMCAs), and Method of Configuring, of which the following is a specification.

DOMINIK & STEIN
Suite 400
3030 N. Rocky Point Drive, W.
Tampa, Florida 33607-5904
Telephone: 813/289-2966

ATTORNEY DOCKET NUMBER: 2115.007

Computer Memory Chip with
Field Programmable Memory Cell Arrays (FPMCAs), and
Method of Configuring

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a programmable computer memory chip and to a method of dynamically configuring the memory chip to different I/O bus widths.

Description of the Background Art

As shown in Fig. 1, conventional computer random access memory (RAM) chip 10 contains a memory array 12 having memory cells that can each be individually addressed by a row decoder 14 and a column decoder 16 to input or output data by means of I/O circuits 18 and input and output data control circuits 20 and 22, respectively as determined by chip select/write enable logic, generally indicated by numeral 24. Most of these chips 10 organize the memory cells in a matrix fashion and employ a decoding scheme utilizing the row and column decoders 14 & 16. More particularly, approximately one-half the address lines 26 are decoded by the row decoder 14 and the remaining address lines 28 are decoded by the column decoder 16.

For example, a 1Mb (megabits of memory) X 1 (word width of 1) chip has 1048576 cells divided into 1024 rows and 1024 columns. There are 20 address lines, 10 of which are used to

select one of the 1024 rows of memory cells. The remaining 10

bits are used as column address inputs to select one of the 1024

columns. The row decoder 14 has 10 inputs and 1024 outputs. The

column decoder also has 10 inputs and 1024 outputs. For any

specific address, only one of the 1024 rows and only one of the

1024 columns will be activated, and only one cell gets active row

and column address and the output of that cell will appear at the

memory output. The I/O circuit 18 permits a stored bit to be

output to the data output pin 22 during a read and to be changed

by the input 20 from the data during a write. In dynamic RAMs,

the I/O circuits 28 will include sense amplifiers, etc.

Several innovative static RAM (SRAM) and dynamic RAM (DRAM)

architectures have been proposed recently, examples being fast

static RAMs from Motorola such as BurstRAMs and DSPRAMs, the

cached DRAM from Mitsubishi and Ramtron, the synchronous DRAM

from the Joint Electron Devices Engineering Council (Jedec) and

in the Rambus and Ramlink architectures (B. Prince, "Memory in

the fast lane", IEEE Spectrum, Feb. 1994, pp. 38-41; W. J. Hsieh,

"Reconfigurable Hardware", Computer Design, March 1993, pp.

27-30). The key feature in many of these architectures is that

the I/O architecture of a RAM is modified so that rapid bursts of

data may issue from the internal RAM bus without having to wait

2

the entire access cycle. RAMs are often built as a square or rectangular array of cells, and the processor first sends a row address and then a column address to specify the cell address. To raise their operating mode, DRAMs have a special operating mode that takes advantage of the internal row-and-column structure, known as the page mode (B. Prince, "Memory in the fast lane", IEEE Spectrum, Feb. 1994, pp. 38-413). In this mode, an entire row is read into the sense amplifiers, the row may be kept active and column addresses changed to access all the data. As long as the accesses remain in the same row, the DRAM can work faster.

The fact that the word width of existing memory chips are fixed, creates a granularity problem in wide-bus memory systems Granularity is the minimum increment of memory that may be added to a system. Personal computers and workstations normally use Single In-line Memory Modules (SIMMs), which are small printed circuit boards stocked with multiple RAM chips arranged in parallel to yield a word width of 32 to 144 bits, matching the memory system word width to the processor's bus width. Hence, memory granularity can sometimes be very troublesome (B. Prince, "Memory in the fast lane", IEEE Spectrum, Feb. 1994, pp. 38-41).

Memory granularity increases as the word width of the memory

3

chip becomes narrower with respect to the memory bus. Quoting the example used by Prince, in a 16-bit wide bus that uses 4Mb DRAMs, if the chips are organized as 1M X 4 bits, then it takes four of them to fill out the 16-bit memory bus with a minimum granularity of 2 MByte (1 Byte = 8 bits) of memory ((1024 x 1024 x 4)bits/chip x 4 chips ÷ 8bits\Byte = 2 MByte). If, however, the memory chip is organized as 4M X 1 bits, then 16 of them are needed to fill out a 16-bit bus with a minimum granularity of 8 MBytes of memory. The width of the chips used thus affects the expandability of the memory system.

It is desirable to be able to configure the memory chip to a different widths. The only known memory chip that is capable of being reconfigured is the Motorola 1M X 4/2M X 2 bit Fast Static RAM memory chip (Part Number MCM101524). This Motorola chip is a 4Mb RAM whose I/O can be electrically reconfigured from a normal configuration as 1M X 4 bits to 2M X 2 bits by applying power supply voltage to a mode select pin on the chip. Unfortunately, no other reconfigurations are possible.

Therefore, it is an object of this invention to provide an improvement which overcomes the aforementioned inadequacies of the prior art memory chips and provides an improvement which is a significant contribution to the advancement of the memory chip

4

art.

Another object of this invention is to provide a memory chip of N cells that may be dynamically reconfigured to N X 1 bit, N/2 X 2 bits, N/4 X 4 bits or in general, N/k X k bits, where k is a power of two.

Another object of this invention is to provide a new and useful method for dynamically reconfiguring a computer memory chip of N cells to N X 1 bit, N/2 X 2 bits, N/4 X 4 bits or in general, N/k X k bits, where k is a power of two..

The foregoing has outlined some of the pertinent objects of the invention. These objects should be construed to merely illustrative of some of the more prominent features and applications of the intended invention. Many other beneficial results can be attained by applying the disclosed invention in a different manner or modifying the invention within the scope of the disclosure. Accordingly, other objects and a fuller understanding of the invention made be had by referring to the following summary and the detailed description of the preferred embodiment of the invention, taken in conjunction with the accompanying drawings.

5

SUMMARY OF THE INVENTION

For the purpose of summarizing this invention, this invention comprises a new and useful computer memory chip, referred to herein as a Field Programmable Memory Cell Array (FPMCA) chip. The FPMCA chip of the invention includes a plurality of memory cells in a predetermined arrangement, a programmable address decoder to enable the memory cells to be addressed and a programmable interconnect having a plurality of programmable connection devices to enable the I/O to be interfaced to a processor. According to one preferred embodiment, the programmable address decoder comprises multiplexers and decoders for addressing the memory cells of the chip and the programmable connection devices comprises PASS transistors for reconfiguring the I/O of the chip.

A method for configuring a computer memory chip, according to the present invention, comprises providing a FPMCA chip as described above, and programming the programmable address decoder and the connection devices as described above so as to reconfigure the arrangement of the memory cells to a selected configuration, and to configure the control logic to interface the memory cells in that selected configuration to a processor in a predetermined manner.

6

The FPMCA chip of the invention, and the corresponding method for reconfiguring the FPMCA chip, achieves the desired objective of providing a memory chip of N cells that may be dynamically reconfigured to N X 1 bit, N/2 X 2 bits, N/4 X 4 bits or in general, N/k X k bits, where k is a power of two.

The FPMCA chip of the invention will therefore add more flexibility to all uses of memory chips. Memory manufacturers need not make X1, X4, X16 and X32 chips. Only one generic array need be manufactured, and then the generic memory array can be easily programmed to the desired configuration.

Additionally, FPMCA chips of the invention can be used as variable-width memory chips, dynamically configurable caches, dynamically alterable interleaving schemes and other reconfigurable memory architectures.

Accordingly, it should be appreciated that the design of the programmable circuitry allows the use of the FPMCA chip in a variety of different modes since the FPMCA chip can be reconfigured to several different widths and can be interfaced to different processors with different bus widths.

The foregoing has outlined rather broadly the more pertinent and important features of the present invention in order that the detailed description of the invention that follows may be better

7

understood so that the present contribution to the art can be more fully appreciated. Additional features of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the nature and objects of the invention, reference should be had to the following detailed description taken in connection with the accompanying drawings in which:

Fig. 1 is a block diagram illustrating the organization of a typical memory chip according to the prior art;

Figs. 2A, B and C are block diagrams illustrating the use of a PASS transistor, transmission gate and multiplexer for reconfigurable interconnect according to the prior art;

Fig. 3 is a block diagram illustrating a fully programmable memory cell array according to the present invention in which a sea-of-memory-cells along with a programmable interconnect is present inside the chip;

Fig. 4 is a block diagram illustrating the design of a FPMCA chip according to the present invention, with programmable column decoder and data width;

Fig. 5 is a block diagram illustrating the programmable address decoders of the invention as including demultiplexers and decoders; ;

Fig. 6 is a logic chart illustrating the input and outputs of the control logic in Fig. 5A;

Fig. 7 is a decoding chart illustrating the generation of select signals for the multiplexers of Fig. 5A from three mode pins;

Fig. 8 is a schematic diagram illustrating the programmable connection devices for reconfiguring the I/O width of the FPMCA chip of the invention;

Fig. 9 is a block diagram listing the values for the select signals to the programmable I/O controller for achieving five different configurations of the FPMCA chip of the invention; and

Fig. 10 is a decoding chart illustrating how address pins can be combined with mode pins to minimize the number of necessary pins on the FPMCA chip of the invention.

Similar reference characters refer to similar parts throughout the several views of the drawings.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

As shown in Fig. 1, the field programmable memory cell array (FPMCA) chip 30 of the invention conventionally comprises, as described above, a memory array 12 addressed by a row decoder 14 and a column decoder 16 to input or output data by means of I/O circuits 18 and input and output data control circuits 20 and 22, respectively, as determined by chip select/write enable logic, generally indicated by numeral 24.

The inventive concept of the FPMCA chip 30 of the invention is the inclusion of a programmable address decoder 32 (see Fig. 5) and programmable interconnect 34 (see Fig. 8) that allow selective reconfiguration of the sea of N memory cells 36 (see Fig. 3) of the FPMCA chip 30 to N X 1 bit, N/2 X 2 bits, N/4 X 4 bits or in general, N/k X k bits, where k is a power of two.

Fig. 4 is a block diagram of one embodiment of the FPMCA chip 30 according to the present invention. The FPMCA chip 30 has a hard-wired or rigid row decoder 14 and has a column decoder 16 that comprises the programmable address decoder 32 of the invention. Those skilled in the art will realize that several designs allowing for different levels of programmability in either row or column decoder or both can be realized by incorporating the principles of the present invention.

11

For purposes of explaining the present invention, a 1M X 1 bit chip is assumed. When the word width is increased to double the existing width, the number of address lines is reduced by one. Thus, when the word width increases k times, the number of address lines gets reduced by log(k). The reconfigurable FPMCA chip 30 supports the number of data pins corresponding to the largest width to be supported and the number address pins corresponding to the smallest width. In the embodiment in Fig. 4, assume that the 1M X 1 bit chip is to be reconfigurable to 512K X 2 bits, or 256K X 4 bits, or 128K X 8 bits, or 64K X 16 bits. In the different configurations, 20, 19, 18, 17, or 16 address pins and 1, 2, 4, 8, 16 data pins respectively, are required. The twenty address pins are designated A0, A1, A2,...A19. The lower 10 address pins A0, A1,...A9 are connected to the row decoder 14. The higher 10 address bits, A10, A11,...A19 are connected to the column decoder 16. The row decoder 14 is hardwired, so it will always have 10 address bits. The column decoder 16 will use 10, 9, 8, 7, and 6 bits when the word width of the chip is 1, 2, 4, 8, and 16 bits respectively.

The purpose of the programmable address decoder 32 and the programmable interconnect 34 is to configure the word width to the desired width and correspondingly configure the column

12

decoder, column address pins and data pins.

Programmable Address Decoder

The programmable address decoder 32 of the invention comprises four mode control lines 38 (MC1,...MC4) connected to the control inputs 40 of four paired demultiplexers 42 (see Fig. A of Fig. 5 and also Fig. 2C). The data input 44 of one of each paired demultiplexers 42 is respectively connected to the four column address lines 28 (A16,...A19) and the data input 46 of the other of each paired demultiplexers 42 is respectively connected to the complement of such column address lines 28 ($\overline{A}16,...\overline{A}19$). The other data inputs 48 of each of the demultiplexers 42 are held high H.

The output terminals 50 (labeled a0, $\overline{a}0$,...a3, $\overline{a}3$ for convenience) of the demultiplexers 42 are logically connected as indicated in Fig. B of Fig. 5 to the enable inputs 52 of sixteen 6X64 decoders 54. The remaining six column address lines 28 (A10,...A15) are respectively connected to the six inputs 56 of the each of the sixteen decoders 54. The 1024 outputs 58 of the sixteen 6X64 decoders 54 (16 x 64 = 1024) are respectively connected to the columns 36C of the memory array 12.

It is noted that since there are sixteen 6X64 decoders 54 and since they are enabled depending upon the logic state of the

13

four mode control lines 38, only 1, 2, 4, 8 or 16 of such

decoders 54 will be enabled at any one time. Further, since only

one of the outputs 58 of the enabled decoders 56 may will high

depending upon the respective inputs 56, only 1, 2, 4, 8, or 16

columns 36C of the memory array 12 are addressed. With 1, 2, 4,

8, or 16 columns of the memory cells 36 being addressed, the word

length of the FPMCA chip 30 may be 1, 2, 4, 8, or 16 bits wide

(see the logic table of Fig. 6).

Since there are five different modes to be supported, at

least three external mode pins are required for mode control.

More specifically, as shown in the logic table of Fig. 7, the

three external mode pins (M1, M2, M3) may be translated by

suitable logic 60 (see Fig. 5), to the four mode control lines

(MC1, MC2, MC3, MC4).

Programmable Interconnect

Referring now to Fig. 8, the output circuitry of the 16-bit

wide FPMCA chip can be programmed to 8, or 4, or 2, or 1 bit word

widths by means of a PASS transistors 62 (see Fig. 2A) or a

transmission gate 64 (see Fig. 2B), or other suitable switch.

More particularly, PASS transistors 62 are placed between the

data lines 66 of the I/O circuits of the FPMCA chip 30 so that

they can be connected together or not, depending on the desired

14

word width. As illustrated, four levels of PASS transistors are required to change the word width to include 1, 2, 4, 8 and 16 widths.

In general, log(k) levels of PASS transistors 62 are required for varying the word width to k times. In fact, all of the PASS transistors 62 in any one level will be having identical contents. This principle may be used to reduce the number of mode control lines used in the circuit. The PASS transistors 62 can be programmed to the aforementioned level of flexibility by log(k) control lines, one for each level of PASS transistors 62.

Fig. 8 illustrates the manner in which sixteen data lines 66 can be controlled by the four mode control lines 38 (described above in connection with the programmable address decoder 32) to yield any word width from 16, 8, 4, 2 to 1, which are powers of two. Fig. 9 illustrates the values required to control the PASS transistors 62. It is noted that a circuit similar to Fig. 8 has to be incorporated into the input circuitry also. The mode control lines 38 controlling the PASS transistors in the input data lines can be the same as those in the output circuitry.

At this point it is noted that the mode control lines 38 for the programmable address decoder 32 has identical values as the mode control lines for word-width adjustment and hence the same

15

lines may be used. The mode control lines could be replaced by a

mode control register built of static RAM cells (as in Xilinx

FPGAs). In an embodiment that uses the static RAM cells to

control the chip width, the values in the static RAM cells will

correspond to Fig. 9.

Looking at the values on the mode control lines 38 as in

Fig. 9, it can be seen that out of the 16 possible values for the

4 mode control lines, only 5 are being used. In general, out of

all possible k combinations of contents for the log(k) select

lines, only log(k) + 1 combinations are being used. Hence the

number of control lines may be minimized to log (log(k) + 1).

Thus just 3 lines are sufficient for programming from 1 bit to 16

bit. From 3 lines, the four control signals can be generated

according to Fig. 7. Even in a case for programming from 1 bit

to 1024 bit width, all that is required is 4 lines.

Finally, as shown in Fig. 10, the log (log(k) + 1) lines or

4 control lines in the embodiment in Fig. 4 can be overlapped

with the address bits. Specifically, each increase in the data

width by k times, reduces the number of address lines required by

log(k). Those lines can be shared to deliver the mode

information to the chip. Fig. 10 illustrates the manner in which

the address lines and the mode control bits can be shared. Only

16

one extra line will be required to indicate the mode. That line
if 0 commands the chip to be in the narrowest possible
configuration. If the line is 1, the chip is in a wider mode.
Hence at least the highest address line A20 is not required for
addressing. So A20 can be used for mode information. If A20 is
0, the chip is twice as wide as the narrowest configuration. If
A20 is a 1, the chip is even wider. So A19 is not required for
addressing and will be used for mode information. If A19 is 0,
the chip is 4 times as wide as the narrowest configuration. If
A19 is 1, the chip is wider than 4 times the original width. So
A18 will not be required for addressing and can be used for mode
information. If A18 is a 0, the chip is 8 times the original
width and if A18 is a 1, the chip is 16 times the original width.
Thus mode control can be accomplished by just one extra pin.
Even that one pin can be overlapped with some of the data pins.

The present disclosure includes that contained in the
appended claims, as well as that of the foregoing description.
Although this invention has been described in its preferred form
with a certain degree of particularity, it is understood that the
present disclosure of the preferred form has been made only by
way of example and that numerous changes in the details of
construction and the combination and arrangement of parts may be

17

resorted to without departing from the spirit and scope of the invention.

Now that the invention has been described,

WHAT IS CLAIMED IS: